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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/650,661	08/29/2003	Takao Moriwaki	402767	7786	
23548	7590 11/30/2004		EXAM	EXAMINER	
LEYDIG VOIT & MAYER, LTD 700 THIRTEENTH ST. NW			NGUYEN, KHANH V		
SUITE 300	ENTH ST. NW		ART UNIT	PAPER NUMBER	
WASHINGTO	N, DC 20005-3960		2817		
			DATE MAILED: 11/30/200-	4	

Please find below and/or attached an Office communication concerning this application or proceeding.

•	Application No.	Applicant(s)				
	10/650,661	MORIWAKI ET AL.				
Office Action Summary	Examiner	Art Unit	1			
	Khanh V. Nguyen	2817	Jan Jan			
The MAILING DATE of this communication app Period for Reply		·	ess			
A SHORTENED STATUTORY PERIOD FOR REPL' THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.1: after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply If NO period for reply is specified above, the maximum statutory period Failure to reply within the set or extended period for reply will, by statute Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	36(a). In no event, however, may a reply y within the statutory minimum of thirty (3 vill apply and will expire SIX (6) MONTHS , cause the application to become ABANI	be timely filed 0) days will be considered timely. 3 from the mailing date of this comm DONED (35 U.S.C. § 133).	nunication.			
Status						
1) Responsive to communication(s) filed on 29 A	ugust 2003.					
2a) ☐ This action is FINAL . 2b) ☑ This	action is non-final.					
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is						
closed in accordance with the practice under E	Ex parte Quayle, 1935 C.D. 1	1, 453 O.G. 213.				
Disposition of Claims						
4) Claim(s) 1-4 is/are pending in the application.						
4a) Of the above claim(s) is/are withdraw	wn from consideration.					
5) Claim(s) is/are allowed.						
	S)⊠ Claim(s) <u>1-4</u> is/are rejected.					
7) Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and/o	r election requirement.					
Application Papers						
9)☐ The specification is objected to by the Examine	r.					
10) ☐ The drawing(s) filed on is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.						
Applicant may not request that any objection to the						
Replacement drawing sheet(s) including the correct 11) The oath or declaration is objected to by the Ex						
Priority under 35 U.S.C. § 119		_				
12)⊠ Acknowledgment is made of a claim for foreign a)⊠ All b)☐ Some * c)☐ None of:	priority under 35 U.S.C. § 1	19(a)-(d) or (f).				
1.⊠ Certified copies of the priority document	s have been received.					
2. Certified copies of the priority document	• •					
3. Copies of the certified copies of the prio		ceived in this National St	age			
application from the International Burea	,	noived				
* See the attached detailed Office action for a list	or the certified copies not rec	Selveu.				
Attachment(s)						
Attachment(s) 1) Notice of References Cited (PTO-892)	4) 🔲 Interview Sum	nmary (PTO-413)				
 Notice of Netericles Cited (PTO-032) Notice of Draftsperson's Patent Drawing Review (PTO-948) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>8/29/03</u>. 	Paper No(s)/N	Mail Date rmal Patent Application (PTO-1	52)			

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2 stated "the semiconductor element is a transistor" but there is no drawing Figure shown having such a transistor. It is noted that Figure 1 of the application shows a "semiconductor element" which is a resistor.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Baro (3,896,394).

Baro disclose an amplifier circuit comprising: a transistor (Q3) can be read as a semiconductor amplification element; a transistor (Q2) can be read as a bias circuit; and a power source (Vo) of the bias circuit is connected to a power source (Vo) of transistor (Q3) via resistor (R9), as such any changes to a supply voltage of transistor (Q3) will have the same effect in the idle current.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baro.

Baro disclosed the claimed invention except the semiconductor element is a transistor/diode. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced a resistor (R9) of Baro with a transistor/diode, since such a substitution is well known in the art based on the intended use of the invention (see U.S. Patent **5,777,517**).

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita (6,731,171) in view of Bailey et al. (5,654,672).

Regarding claim 1, Yamashita (Fig. 2) disclose the claimed invention except a power source (1) of the bias circuit (52) is connected to a power source (1) of the semiconductor amplification element (10) via a semiconductor element.

Bailey et al. (Fig. 3) disclose a bias circuit (22) comprises a bias transistor (31) connected to a power source (VCC) via resistor (33).

Accordingly, it would have been obvious in view of the reference, taken as a whole, to have modified the circuit of Yamashita to have included a resistor having the

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connection thereof, as taught Bailey et al. Such a modification would have imparted the advantageous benefit of reduced the power dissipation of the bias transistor (see col. 5, lines 43-47) as taught by Bailey et al., to Yamashita reference, thereby suggesting the obviousness of such a modification.

Regarding claims 2, 3, Yamashita and Bailey combined disclosed the claimed invention except the semiconductor element is a transistor/diode. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced a resistor of Yamashita and Bailey with a transistor/diode, since such a substitution is well known in the art based on the intended use of the invention (see U.S. Patent 5,777,517).

Regarding claim 4, wherein transistor (52) of Yamashita (Fig. 2) can be read as a bias generating circuit for generating a base bias of the high-frequency transistor (10) and diode connected transistors (50, 51) can be read as a temperature compensation circuit having the function thereof.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The additional reference (Brayton et al. (6,046,642) shows further analogous prior art circuitry.

This art is deemed relevant and should be carefully reviews before any amendment is filed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh V. Nguyen whose telephone number is (571) 272-1767. The examiner can normally be reached from 8:00 AM - 3:30 PM EST.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KHANH V. NGUYEN
PRIMARY EXAMINER

Maul Oardquyer

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